



Digital Semiconductor SA-110 Microprocessor

Product Brief

Description

The Digital Semiconductor SA-110 microprocessor (SA-110) is the first member of the StrongARM family of high-performance, low-power microprocessors. The SA-110 is the latest implementation of Advanced RISC Machines Ltd. (ARM) Version 4 architecture and offers significant advances in microprocessor design. The SA-110 has been designed to further extend the ARM family as the world's leading source of low-power, high-performance RISC processors for embedded consumer markets such as smart hand-held devices and interactive digital video.

The SA-110 is a general-purpose, 32-bit microprocessor with a 16KB instruction cache (Icache); a 16KB, write-back data cache (Dcache); a write buffer; and a memory-management unit (MMU) combined in a single chip. The five-stage pipeline distributes tasks evenly over time to remove bottlenecks, ensuring high throughput for the core logic. The SA-110 offers high-level RISC performance, yet it ensures minimal power consumption, making it ideal for portable, low-cost systems.

The SA-110 onchip MMU supports a conventional 2-level page-table structure, with a number of extensions, which makes it ideal for embedded control systems and object-oriented systems. These features result in a high instruction throughput and impressive real-time response for a small and cost-effective chip.

Features

- Internal clock nominal frequencies
 - 100 MHz @ 1.65 V
 - 160 MHz @ 1.65 V
 - 200 MHz @ 2.0 V
- High-performance benchmarks (est.)
 - 115 V2.1 Dhrystone MIPS (100)
 - 185 V2.1 Dhrystone MIPS (160)
 - 230 V2.1 Dhrystone MIPS (200)
- Onchip phase-locked loop (PLL) referenced from a 3.68-MHz external oscillator
- Five-stage pipeline sequences tasks evenly for high performance
- MMU support for virtual memory systems
- Write buffer to improve system performance
- Onchip, 32-way, set-associative cache
 - 16KB instruction cache
 - 16KB write-back data cache
- Big and little endian operating modes
- Static operation with low power use
- 3.3 V I/O interface with independent programmable bus clock
- Power-down modes: idle and sleep
- Fast interrupt response—less than 1 μ s for real-time applications
- Excellent support for high-level languages, including exceptional code density
- Support for IEEE 1149.1 test interface port
- Packaged in a 144-pin thin quad flat pack (TQFP)

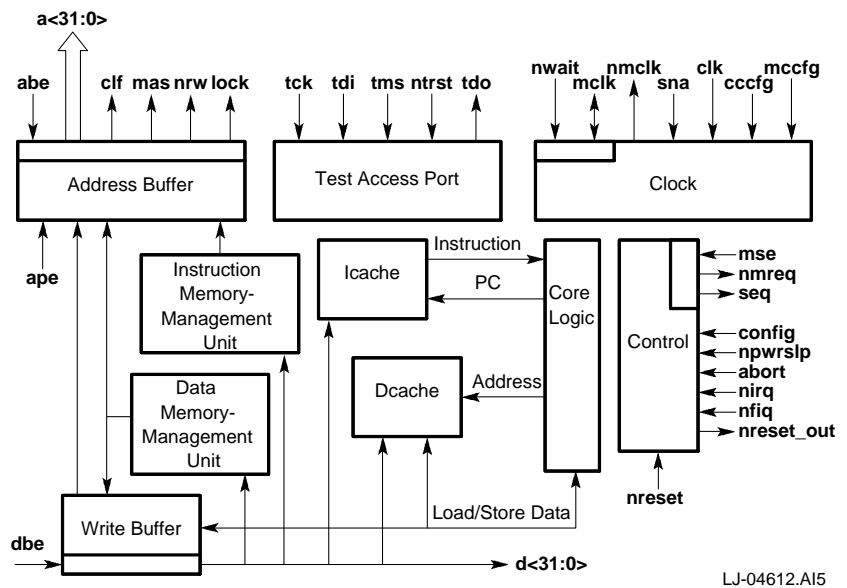
Applications

- Smart hand-held devices
 - Personal digital assistant (PDA)
 - Next-generation cellular telephone
 - Organizer
 - Pager
- Video conference equipment
- High-performance real-time systems
 - Disk drives
 - Data communications equipment
- Interactive digital video
 - Video games
 - Internet browsers
 - Set-tops

Microarchitecture

The SA-110 microprocessor is a high-performance implementation of Advanced RISC Machine's ARM Version 4 architecture specification. Figure 1 shows a block diagram of the SA-110.

Figure 1 Block Diagram of the SA-110



The following sections provide an overview of the chip's microarchitecture and major functional units.

Bus Interface Logic

The bus interface logic, consisting of the control logic and the address register, controls the bus interface and unplanned events such as interrupts, resets, and aborts. The bus interface logic can also enable or disable wrapping of read transactions and merging of write transactions.

The bus interface can be configured to run synchronously or asynchronously to the core logic. In synchronous mode, the bus interface clock speed is the core clock rate divided by a programmable integer value from 2 to 9 (maximum of 66 MHz). In asynchronous mode, the bus interface clock, from 1 MHz to 66 MHz, is supplied by an external source.

Write Buffer

The SA-110 has an 8-entry write buffer with each entry able to contain 1 byte to 16 bytes. The write buffer can be enabled or disabled by software. The write buffer is further controlled by a bit in the MMU page tables; so the MMU must be enabled before the write buffer can be used. Software can cause the write buffer to be flushed.

Core Logic

The core logic fetches and executes instructions by using a five-stage pipeline. The five stages are: fetch, decode, arithmetic logic unit (ALU), cache, and write-back. This pipeline arrangement, using the onchip ALU, distributes tasks evenly in time and so contributes to the high performance of the core logic.

The ARM architecture supports 30 general-purpose registers, 1 program counter, and 6 status registers. There are 16 general-purpose registers (including the PC register) and 1 or 2 status registers visible at any one time. The processor operating mode determines which registers are visible.

The core logic executes the ARM instruction set, which supports straight-forward assembly language code programming. It does not depend upon sophisticated compilers to manage complicated instruction interdependence. The instruction set has eight instruction classes:

- Two instruction classes use the onchip ALU, barrel shifter, and multiplier to perform high-speed operations on the data in a bank of 16 logical (31 physical) 32-bit registers.
- Three instruction classes control data transfer between memory and the registers. The classes are optimized for flexible addressing, rapid context switching, and swapping data.
- Two instruction classes control execution flow and execution privilege level.
- One instruction class accesses the privileged state of the SA-110.

The core logic implements 32-bit virtual addresses and 32-bit physical addresses. A 12-bit multiplier with early termination performs multiplication. The number of cycles needed to perform a multiplication operation depends on the magnitude of the operands, as shown in Table 1.

Table 1 Core Logic Multiplication Functions

Multiplication Operation (Signed or Unsigned)	Result Size	Operation Duration
32 x 32	32 bits	2–4 cycles
32 x 32 + 32	32 bits	2–4 cycles
32 x 32	64 bits	3–5 cycles
32 x 32 + 64	64 bits	3–5 cycles

Memory-Management Units

The SA-110 has two memory-management units: instruction (IMMU) and data (DMMU). Separate translation lookaside buffers (TLBs) are implemented for the instruction and data streams. The TLBs each have 32 entries that can each map a segment, a large page, or a small page. The TLB entry replacement algorithm is round-robin. The data TLB supports both the flush-all and the flush-single-entry function, while the instruction TLB supports only the flush-all function. Memory-management exceptions preserve the base address registers, eliminating the need for “fix-up” code.

Cache

The SA-110 has a 16KB, 32-way, set-associative Icache with 32-byte blocks and a 16KB, 32-way, set-associative, write-back Dcache with 32-byte blocks.

Instruction Cache

The Icache supports the flush-all-entry function, and the replacement algorithm is round-robin within a set. The Icache can be enabled or disabled independent of the memory-management function. When memory management is disabled, the Icache control logic considers all memory to be cacheable.

Data Cache

The write-back Dcache supports the flush-all-entry, flush-entry, and copy-back-entry functions. The copyback-all function is not provided in hardware but can be provided by software. The Dcache entries are allocated with read transactions and the entry replacement logic uses a round-robin algorithm.

Clocks

The SA-110 receives a 3.68-MHz clock from a crystal-based clock generator. The SA-110 uses an internal phase-locked loop (PLL) to multiply the frequency by a variable multiplier to produce a high-speed clock. The high-speed clock is then divided internally by a configurable ratio to provide a system clock for synchronous operation. The 3.68-MHz oscillator and PLL run constantly in normal and idle mode.

Boundary-Scan Test Logic

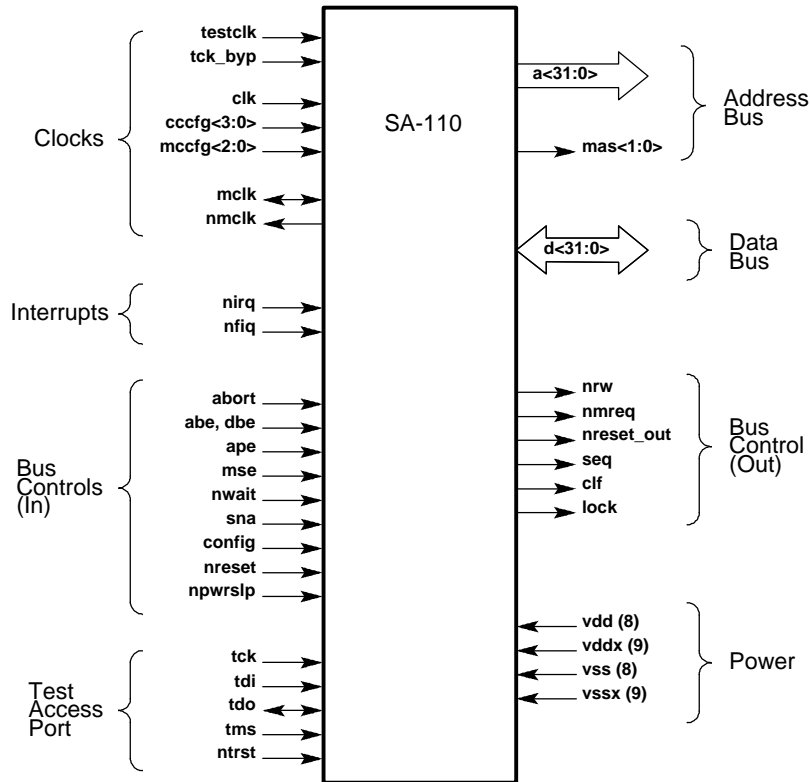
The SA-110 boundary-scan interface provides for driving and sampling all the external pins of the device except **npwrslp**, irrespective of the core logic state. This ability permits testing of:

- SA-110 electrical connections to the circuit board
- Integrity of connections between devices having a similar interface on the circuit board

Signal Lines

Figure 2 shows the signal connects to and from the SA-110. The signals are arranged within functional groups.

Figure 2 Functional Group Signal Lines



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SA-110 Characteristics

Characteristic	Specification
Core power supply	vss = 0.0 V dc vdd = 1.65 V dc ±10% or 2.0 V dc ±10%
I/O power supply	vssx = 0.0 V dc vddx = 3.3 V dc ±10%
Operating temperature	T _j = 100°C (212°F)
Storage temperature range	-40°C to +125°C (-40°F to +257°F)
Normal operation mode	< 300 mW @ 100 MHz (1.65 V dc) < 450 mW @ 160 MHz (1.65 V dc) < 900 mW @ 200 MHz (2.0 V dc)
Idle mode	< 20 mW mclk is off, PLL is on
Sleep mode	< 50 µA vdd is off, PLL is off, O and I/O pins are driven to a zero deasserted state
Package Process technology Transistor count Die size	144-pin TQFP 0.35 µm, 3-layer metal 2.1 million 50 mm ²

For More Information

To learn more about the availability of the SA-110 microprocessor, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

United States and Canada
1-800-332-2717
Outside North America
1-508-628-4760

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